AMENDMENT TO THE SPECIFICATION

Amend the paragraph beginning at page 3, line 22 as follows:

Clock generator 110 generates an output 116 having a frequency that is a multiple, *m*, of the frequency of a reference clock, REFCLK 112. In the illustrated embodiment, clock generator 110 is a phase locked loop (PLL). The PLL has a feedback path including inverter ~~182~~ 172, divider 170, and flip-flop 150.

Approved 9/12/05

Amend the paragraph beginning at page 8, line 21 as follows:

Figure 5 thus illustrates a clock generator providing a clock output 514 having a frequency that is twice that of a received reference clock 512. A multiplexer 530 is coupled to select one of the clock output 514 and a gated clock 520 output as a double clock 516 in accordance with a halt multiplexer control 546. Divider circuitry 570 divides the double clock to provide an alignment signal 576 with a frequency half that of the double clock. A recovery circuit 598 recovers a first clock 580A and a second clock 590A from the double clock 516 in accordance with the alignment signal 576, wherein the first and second clocks have substantially a 90° phase difference.

Amend the paragraph beginning at page 8, line 30 as follows:

The halt control should be disabled during normal operation. This is accomplished in one embodiment by tying HALT 542 to a logic level that ensures halt multiplexer control 546 always selects PLL output 514 during normal operational modes. Stop level 544 indicates the logic level at which the halt should occur as further described with respect to Figure 6.

Amend the paragraph beginning at page 11, line 6 as follows:

The integrated circuit die 830 resides within an integrated circuit package 820. A REFCLK 812 is provided to the clock generator 830 via an external pin 822 of the integrated circuit package 820.